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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,046	01/09/2007	Fung Leng Chen	Q74738	6904

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EXAMINER	
KUSUMAKAR, KAREN M	

ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
02/01/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/552,046	CHEN ET AL.	
	Examiner	Art Unit	
	KAREN M. KUSUMAKAR	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-11 and 13* is/are rejected.

7)☒ Claim(s) *12 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. The request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e) and a submission, filed on 1/4/10 is accepted.

Status of Claims

2. As of the amendment filed 12/10/09, no claims have been added or cancelled, and claims 1, 2, 10, and 12 have been amended. Therefore, claims 1-2 and 5-16 remain pending, with claims 1, 2, 10, and 12 being independent.

Claim Objections

3. Claim 12 is objected to because of the following informalities: it is unclear to which secondary IC structure (i.e. the first or the second) "substantially planar surface on the underside of **said secondary IC structure**" (line 7 of page 9) is referring. According to figure 7, it appears applicant was referring to said second secondary IC structure. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. Claims 1, 5, 6, 8-10, and 13 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over ***Subraya et al. (US 2007/0210433).***

As to claims 1, 5, 6 and 10, Subraya teaches a ball grid array package (Fig. 3) comprising:

- a base IC structure (51), the base IC structure comprising:

  a base substrate (52) having a first base substrate face (top surface of 52),

  a second base substrate face (57) opposite to said first base substrate face (Fig. 3),

  a base substrate opening (56) extending between said first base substrate face and said second base substrate face (Fig. 3),

  a base conductor (58);

- a first semiconductor chip (54), comprising:

  a first chip face (bottom surface of 54),

  a second chip face (top surface of 54) opposite to said first chip face (Fig. 3),

  first bond pads (55) disposed over said base substrate opening (Fig. 3);

  a first plurality of wires (59) disposed to pass through said base substrate opening and electrically connecting said first bond pads to said base conductor (Fig. 3, p. 3, [0032]);

- a secondary IC structure (71), comprising:

  a second substrate (72) having a first secondary substrate face (80),

  a second secondary substrate face (bottom surface of 72) opposite to said first secondary substrate face (Fig. 3),

a secondary opening (76) extending between said first secondary substrate face and said second secondary substrate face, and a secondary conductor (Fig. 3);

- a second semiconductor chip (74), comprising:

  a first secondary chip face (bottom surface of 74),

  a second bond pad (75) disposed over said secondary opening (76, Fig. 3); and

  a second plurality of wires (79) electrically connecting said second bond pads to said secondary conductor through said secondary opening (Fig. 3, p. 3, ([0032]);

- a first encapsulant (90) filling said secondary opening (76) around said second plurality of wires (79) and covering said second secondary substrate face (bottom surface of 72), wherein said first encapsulant provides a structure that enables mounting of said secondary IC structure on said base IC structure (Fig. 3, [0028], mold 90 fills in the voids and air spaces between the two chips and thus enables mounting. That is, if one were to remove the ball bonds 81 (fig. 3), the mold 90 would still provide mounting support); and
- a third plurality of wires connecting said secondary IC structure to said base IC structure (it is inherent that there is an electrical connection between the secondary IC structure and the Base IC structure. The use of “wires” is either inherent (balls 81 can be considered to be wires) or obvious (wires and balls

and pads are obvious variants of each other)); wherein said secondary IC structure is mounted on said base IC structure (Fig. 3).

As to claim 8, Subraya further teaches at least one additional of said secondary IC structure mounted over said first secondary chip face (Figs. 1 and 2, p. p. 3, [0030]); and respective wires connecting a conductive portion of said at least one additional secondary IC structure to said base IC structure (Each of the IC structures are electrically connected using some sort of electrical contact (wires are an obvious choice), thus the additional IC structure is connected to the base structure either directly or indirectly).

As to claim 9, Subraya further teaches a thermal dissipation element disposed over said first secondary chip face (p. 3, [0033]).

As to claim 13, Subraya further teaches encapsulating at least part of the base IC structure and the first secondary IC structure (Fig. 3, p. 2, [0028]).

5. Claims 1, 7, 10, and 11 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over ***Lee et al. (US 7,005,316).***

As to claims 1, 7, and 10, Lee teaches a ball grid array package (see title and abstract) comprising:

- a base IC structure (110), the base IC structure comprising:

  a base substrate (120) having a first base substrate face (122)

  a second base substrate face (124) opposite to said first base substrate face (Fig. 1a),

a base substrate opening (126) extending between said first base substrate face and said second base substrate face (Fig. 1a),

a base conductor (col. 5:21-26);

- a first semiconductor chip (130), comprising:

  a first chip face (top surface of 130),

  a second chip face (bottom surface of 130) opposite to said first chip face (Fig. 1b),

  first bond pads (pads on active surface 132) disposed over said base substrate opening (Fig. 1a);

  a first plurality of wires (140) disposed to pass through said base substrate opening and electrically connecting said first bond pads to said base conductor (Fig. 1a, col. 5:21-26),

- a secondary IC structure (110'), comprising:

  a second substrate (120') having a first secondary substrate face (124'),

  a second secondary substrate face (122') opposite to said first secondary substrate face (Fig. 1b),

  a secondary opening (126') extending between said first secondary substrate face and said second secondary substrate face, and a secondary conductor (Fig. 1b);

- a second semiconductor chip (130'), comprising:

  a first secondary chip face (top surface of 130), said first secondary chip face is free of said molding compound (Fig. 1d),

a second bond pad (pads on active surface 132) disposed over said secondary opening (Fig. 1b); and

a second plurality of wires (126') electrically connecting said second bond pads to said secondary conductor through said secondary opening (Fig. 1b, col. 5:21-26);

- a first encapsulant (170) filling said secondary opening (126') around said second plurality of wires (140') and covering said second secondary substrate face (122'), wherein said first encapsulant provides a structure that enables mounting of said secondary IC structure on said base IC structure (Fig. 1d, mold 170 fills in the voids and air spaces between the two chips and thus enables mounting. That is, if one were to remove the ball bonds 150, the mold 170 would still provide mounting support); and
- a third plurality of wires connecting said secondary IC structure to said base IC structure (it is inherent that there is an electrical connection between the secondary IC structure and the Base IC structure. The use of "wires" is either inherent (balls 150 can be considered to be wires) or obvious (wires and balls and pads are obvious variants of each other, and Figs. 3 and 4 of Lee teaches reducing the height of the stack as much as possible)); wherein said secondary IC structure is mounted on said base IC structure (Fig. 1d).

As to claim 11, Lee further teaches said encapsulating step comprises first encapsulating said first secondary IC structure (170, col. 6:30-34) and

subsequently encapsulating said base IC structure and said first secondary IC structure, together with said first and second plurality of wires (186, col. 7:37-39).

6. Claim 2 is rejected under 35 U.S.C. 103(a) as obvious over ***Subraya et al. (US 2007/0210433)*** in view of ***Ho (US 2001/0016370).***

As to the beginning part of claim 2, rejection of claim 1 above applies. As to the remaining portion of claim 2, Subraya further teaches: said base substrate further comprises a plurality of vias extending between said first base substrate face and said second base substrate face (Fig. 3) and said base conductor extends through said vias (p. 3, [0033], although the base conductor is not explicitly stated as extending through the vias, conductors are used for making the interconnections between the IC structures and it is very well known to run wiring/plugs through vias, thus it would have been obvious if not inherent to extend the base conductors through the vias so as to connect the structures using as little real estate as possible).

Subraya does not teach said base substrate further comprises a layer of solder mask disposed on portions of said first and second chip faces. However, Ho teaches the use of a solder mask for applications involving wire bonds (p. 4, [0064]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the solder mask of Ho with the base substrate of Subraya so as to protect the device from excessive or misdirected solder.

Allowable Subject Matter

7. Claims 12 and 14-16 are allowable. The following is an examiner's statement of reasons for allowance: The prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitations of the claims listed above in such a manner that a rejection under 35 U.S.C. 102 or 103 would be proper.

In particular, Subraya teaches stacking and electrically connecting a plurality of chips but specifically teaches a single underfill molding step to encapsulate the entire stack. In fact, Subraya specifically states "Different kind of chip arrangements can be used at a time to provide the stacked device as long as the chip arrangements are not encapsulated by a mold or a similar encapsulation material prior to their stacking". Claim 12 states mounting a prior encapsulated chip onto the stack (page 9, line 8 of current amendment), which Subraya specifically teaches against. Thus, it would not have been obvious to modify Subraya to meet these claim limitations.

Lee teaches an underfill molding/encapsulating step in a stacked chip environment, and this step can be performed in two steps (170 and 186, col. 6:30-34 and col. 7:37-40, Fig. 1d). However, Lee teaches these two underfill steps are performed after the substrates have been mounted. Claim 12 (lines 8 and 9 of page 9 of the current amendment) states "Mounting the substantially planar surface of said encapsulant to said first secondary IC structure". That is, claim 12 requires the planar surface to exist prior to mounting. Lee teaches molding/encapsulating after the substrates have been mounted, and thus does not meet this claim limitation.

Claims 14-16 are allowable at least because they depend from claim 12.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

8. Applicant's arguments with respect to claims 1-2 and 5-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any response to this Office Action should be faxed to (571) 273-8300 or mailed to:

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Hand-Delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAREN M. KUSUMAKAR whose telephone number is (571) 270-3520. The examiner can normally be reached on Mon - Thurs 7:30a - 5:00p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. M. K./
Examiner, Art Unit 2829
1/27/2010

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829